europass

Felipe Torres González

Date of birth: 23/01/1991 | **Nationality:** Spanish | **Gender:** Male |

(+34) 691566439 | torresfelipex1@gmail.com | https://github.com/felipet/ |

https://www.linkedin.com/in/felipe-torres-gonzález-70048721b/ |

Other: @felipetg | Navas de Tolosa, 19, 14800, Priego de Córdoba, Spain

About me:
I'm a curious engineer who is always looking for new challenges and stays at the bleeding edge of technology.

My 10-years career has split between Academia and private companies. Different worlds, but a common ground-truth of learnt lessons:

- An awful solution to solve a problem today becomes a big headache sooner or later.
- Perfect solutions might exist, time to find them does not.
- Workmates are more than people that drinks coffee with you.
- Time spent on your workmates is an investment, not a waste of time.
- If you plan to reinvent the wheel, get ready to explain why.

WORK EXPERIENCE

02/2014 – 08/2014
INTERNSHIP – FIDESOL

The main competencies acquired:
- Embedded OS development (Firefox OS) for the SocamFS project (Linux drivers and kernel modules).
- Web development (Razor Franework and C#) for the Ábaco project.
- Data Base development (TSQL) for the Ábaco project.

https://fidesol.org/ | Granada, Spain

10/2014 – 04/2015 – Granada, Spain
RESEARCH FELLOW (PART TIME) – UNIVERSITY OF GRANADA

The main focus of the position was the introduction of synchronization protocols based on Ethernet networks.

The most relevant topics covered were:
- Synchronization protocols (White-Rabbit).
- Embedded system design and development based on Xilinx FPGAs and embedded processors.
- Management and automation of laboratory equipment, such as digital oscilloscopes, time counters, spectrum analyser, etc.

Achievements:
- A tool for the auto-calibration of WR devices: https://github.com/felipet/wrcalibration

Granada

10/2014 – 07/2016 – Granada, Spain
EMBEDDED SYSTEMS ENGINEER – SEVEN SOLUTONS

I was enrolled in the departments of engineering, and production & test of hardware equipment.

The main skills acquired were:

■ Design and development of hardware tests (custom PCBs, FMC based boards, VME based boards, µTCA based boards) using VHDL, C, Python and Bash.
■ Hardware testing and in-house repairment.
■ Data acquisition software development (C and Python).
■ Low-level driver development for the FPGA firmware.
■ Hardware development (VHDL) for Xilinx FPGAs and SoCs.

Link to the open-source library developed within the framework of the hardware tests: https://github.com/felipet/py7slib

http://sevensols.com/ | Granada, Spain

01/12/2015 – 26/08/2018 – Granada, Spain

PHD STUDENT – UNIVERSITY OF GRANADA (UGR)

I enrolled in the timing group at the University of Granada as a result of my interest in the White Rabbit (WR) technology. I strived to increase the number of devices that could be fully synchronized (accuracy below 1 ns) in a daisy-chain network of WR devices.

During my stay, I developed the following skills:

- Increase my knowledge of the PTP protocol, White Rabbit and synchronization networks in general.
- Learn about the characterization of the noise sources of an electronic device and its contribution to the performance of the system. In particular, I used phase noise measurements, and the Allan Deviation (and variants) statistics.
- Developed my knowledge in C programming for embedded devices, sw/hw partitioning, Xilinx's SoC platform, VHDL.
- Use of laboratory equipment such as DSOs, noise analysers, signal generators, and so on.
- Learn about control loops for systems VCXO, PLL and DAC components.
- Established links with other international labs.

My achievements:

- I optimized the control loop of a WR device to achieve up to 22 devices fully connected and synchronized in a row (previously, no more than 10-12 was possible).
- I defined a model to find the maximum number of nodes that could be connected in a row (when using my previous results). The result was about 700 nodes.
- I defined a series of changes to the firmware of the studied device to improve the accuracy of the synchronization for long chains of devices.
- Together with my workmates, I achieved the publication of several scientific papers in high impact journals.

Publications:

- F. Torres-González, J. Díaz, E. Marín-López and R. Rodriguez-Gómez, "Scalability analysis of the white-rabbit technology for cascade-chain networks," 2016 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control, and Communication (ISPCS), 2016, pp. 1-6.
- F. Girela-López, F. Torres-González and J. Díaz, "Ethernet time-transfer based on low frequency white rabbit solution," 2017 Joint Conference of the European Frequency and Time Forum and IEEE International Frequency Control Symposium (EFTF/IFCS), 2017, pp. 186-189.
- F. Girela-López, F. Torres-González and J. Díaz, "Ultra-accurate Ethernet time-transfer with programmable carrier-frequency based on White Rabbit solution," 2017 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control, and Communication (ISPCS), 2017, pp. 1-6, doi: 10.1109/ISPCS.2017.8056745.
- M. Jiménez-López, F. Torres-González, J. L. Gutiérrez-Rivas, M. Rodríguez-Álvarez and J. Díaz, "A Fully Programmable White-Rabbit Node for the SKA Telescope PPS Distribution System," in IEEE Transactions on Instrumentation and Measurement, vol. 68, no. 2, pp. 632-641, Feb. 2019.
- J. L. Gutierrez-Rivas, F. Torres-Gonzalez, E. Ros and J. Diaz, "Enhancing White Rabbit Synchronization Stability and Scalability using P2P Transparent and Hybrid Clocks," in IEEE Transactions on Industrial Informatics.

Granada, Spain

01/09/2018 – 01/09/2021 – Lund, Sweden

EMBEDDED SYSTEMS ENGINEER – EUROPEAN SPALLATION SOURCE

At ESS, I was part of the Hardware & Integration Group for the Integrated Control System division. My scope of work was split in three different areas:

- Development & support of the ESS's fast acquisition platform based on MicroTCA and IOxOS Tosca framework.
- Head of the development and support of the base MicroTCA hardware platform for delivering to system owners in the accelerator.
- Management of the Estonian in-kind contribution to the ESS.

What I achieved:
- I improved the reliability of the IOxOS platform and helped our stakeholders using the platform for their projects.
- I designed and implemented a system for a fast deployment & test of MicroTCA systems.
- I highly improved the overall quality of the Estonian in-kind contribution and achieved the delivery of a useful standalone system that targeted the gap between the slow and the fast control system.
- I made the integration and further development of the open MRF IP core for the delivered system from Estonia.

Link to open-source developed projects:
- https://github.com/felipet/ess-gendev-tools
- https://github.com/icshwi/ess-openevr
- https://github.com/icshwi/mch_config
- https://github.com/felipet/picoEVR

Lund, Sweden

EDUCATION AND TRAINING

09/2010 – 09/2015 – Granada, Spain

UNIVERSITY DEGREE ON COMPUTER SCIENCE WITH MENTION ON COMPUTER ENGINEERING – University of Granada

EQF level 6

09/2016 – 09/2017 – Granada, Spain

MASTER'S DEGREE ON DATA SCIENCE AND COMPUTER ENGINEERING – University of Granada

EQF level 7

LANGUAGE SKILLS

Mother tongue(s): **SPANISH**

Other language(s):

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken production	Spoken interaction	
ENGLISH	B2	B2	B2	B2	B2
FRENCH	A2	A2	A2	A2	A2
RUSSIAN	A1	A1	A1	A1	A1

Levels: A1 and A2: Basic user; B1 and B2: Independent user; C1 and C2: Proficient user

COMMUNICATION AND INTERPERSONAL SKILLS

Communication and interpersonal skills

This is a very important skillset for me, which I always try to improve. I would stress:

- Willness to actively listen and consider all the points of view.
- Self-confidence to discuss when, in my opinion, there is a better way to address a problem.
- Friendly and respectful actitude with colleagues.
- Self-confidence to present results regardless of the target audience.
- Always ready to write reports and document my developments. For me sharing development is a key to success, I always try to ease the understanding of my work. For me is not enough coming to a solution for a problem. If someone needs to continue my work, he should be able to easily understand an continue where I left.

JOB-RELATED SKILLS

Job-related skills

I would like to remark some of my skills that I consider essential to apply this job:

- **8+ years of experience with Xilinx SoC and FPGA** development workflow (Vivado, ISE, SDSoC).
- Advanced level on programming languages for embedded systems: **VHDL, C, assembly**.
- Very good at scripting: **Python and Bash**.
- Good knowledge of **R for data analysis**.
- **Network protocols** (TCP/IP, UDP/IP).
- Very good knowledge of Linux systems and development tools for Linux based systems.
- 8+ years of experience with CVS systems, especially with **Git**.
- Learning the Rust programming language currently.

Other related skills and or remarkable collaborations:

- Collaboration with LNE-SYRTE (Optical frequency group).
- Seminar assistance: Time and Frequency transfer in Optical Fiber by Dr. Per-Olof Hedekvist from SP Technical Institute of Sweden.
- Ph.D course about Statistics applied to research (certificate available if needed)
- Knowledge about the use of oscilloscopes, time counters, and related lab equipment.
- Love to play with real hardware in the lab.